REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the final Office Action dated 30 July 2007. Responsive to the rejections made in the Official Action, Claims 1, 14, 16 and 20-22 have been amended to clarify the combination of elements that form the invention of the subject Patent Application. Claim 13 has been cancelled by this Amendment, as the subject matter thereof appears to be duplicative of subject matter previously incorporated in Claim 1. Claims 12 and 15 were previously cancelled.

In the Official Action, the Examiner rejected Claims 1-3 and 14 under 35 U.S.C. § 103(a), as being unpatentable over Haban, U.S. Patent 6,779,125, in view of Moriyama, U.S. Patent 5,995,552. Claims 4-7 and 16-18 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Haban in view of Moriyama, and further in view of Tian, U.S. Patent 6,624,710. Claims 11 was rejected under 35 U.S.C. § 103(a), as being unpatentable over Haban in view of Moriyama, and further in view of Yamazaki, et al., U.S. Patent 5,398,007. Still further, Claims 8-10 and 19-22 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Haban in view of Moriyama and Tian, and further in view of Yamazaki, et al.

Before discussing the prior art relied upon by the Examiner, it is believed beneficial to first briefly review the structure and method of the invention of the subject Patent Application, as now claimed. The invention of the subject Patent Application is directed to a single crystal oscillator RF transmitter system. The

system includes a microprocessor having a control signal output and a data output for output of digital data to be transmitted, and a converter coupled to the microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system. The system includes a local oscillator responsive to an external crystal for generating a first clock signal having a frequency in a radio frequency band. A clock switch is provided that is coupled to the local oscillator for providing a second clock signal at a lower frequency than the first clock signal to the microprocessor and a third clock signal to the converter. The third clock signal is different in frequency from the first clock signal and the second clock signal. The clock switch has an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal. The RF transmitter system includes a transmitter connected to an output of the converter for receiving the digital packet data and is coupled to the local oscillator for use of the first clock signal as an RF carrier for the digital packet data to be transmitted by the transmitter. Further, the microprocessor, converter, local oscillator, clock switch and transmitter are integrated on a single chip. Thus, the microprocessor provides commands for controlling the operation of the RF transmitter system operation and provides the digital data output that is converted into digital packet data for transmission.

From another aspect, the present invention is directed to a method for transmitting data with an RF transmitter system having a single crystal oscillator and includes a microprocessor connected with a converter that is further in turn connected to a transmitter. The method includes the step of generating a first clock signal at a radio frequency with a crystal oscillator for providing to the transmitter a carrier signal responsive to receipt of a control signal from the microprocessor to start generation of the first clock signal. The method includes the step of generating a second clock signal and a third clock signal by dividing down the first clock signal for respectively providing to the microprocessor and converter clock signals of respectively reduced frequency. Further, the method includes the steps of converting digital data output from the microprocessor into digital packet data by the converter for output to the transmitter, and transmitting the digital packet data modulated on the first clock signal.

From yet another aspect, the present invention is directed to a method for transmitting data with an RF transmitter system having a single crystal oscillator and including a microprocessor connected with a converter that is in turn connected to a transmitter. The method includes the step of generating a first clock signal at a radio frequency with a crystal oscillator responsive to receipt of a control signal from the microprocessor to start generation of the first clock signal. The method includes the steps of generating a second clock signal using an RC oscillator, and generating a third clock signal from the first clock signal output

from the crystal oscillator for coupling to the converter. The third clock frequency is a lower frequency than a frequency of the first clock signal. The method further includes the step of generating a fourth clock signal from the second clock signal for coupling to the microprocessor. The fourth clock signal is a lower frequency than the frequency of the first clock signal and is a higher frequency than the third clock signal. Still further, the method includes the steps of outputting digital data from the microprocessor for transmission by the transmitter, converting the digital data output from the microprocessor into digital packet data by the converter, and modulating the digital packet data with the first clock signal in the transmitter for transmitting an RF signal therefrom.

It is respectfully submitted that the Haban reference is directed to clock generator circuit having a crystal oscillator and a plurality of frequency multipliers for generating additional clock signals at different frequencies. The Examiner admits that the reference fails to disclose a converter coupled to the microprocessor for converting data output from the microprocessor into packets to be transmitted; and a transmitter connected to an output of the converter for receiving the packets and coupled to the local oscillator for use of the first clock signal as an RF carrier for the packets to be transmitted by the transmitter. The Examiner further admits that the reference fails to disclose the microprocessor, converter, local oscillator, clock switch and transmitter being integrated on a chip.

As Haban fails to disclose a converter coupled to the microprocessor for

converting data output from the microprocessor, it is clear that the reference fails to disclose or suggest a microprocessor having a control signal output and a data output for output of digital data to be transmitted, combined with a converter coupled to the microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system, as now claimed. Further, the reference neither discloses nor suggests the clock switch having an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal, as now claimed. Still further, the reference neither discloses nor suggests a transmitter connected to an output of the converter for receiving the digital packet data and being coupled to the local oscillator for use of the first clock signal as an RF carrier for the digital packet data to be transmitted by the transmitter, as claimed. Additionally, Haban does not disclose or suggest the microprocessor signaling the crystal oscillator to stop generating the first clock signal, the converter to shut down or the transmitter to shut down, after the RF signal is transmitted, as now claimed.

The Moriyama reference does not overcome the deficiencies of Haban. The Moriyama reference is directed to radio equipment for communicating digital data. The transmission portion (Fig. 3) includes a baseband part for processing digital data and a transmission part for modulating a radio signal by the digital data and transmitting the modulated signal. An input speech signal is coupled to a data

processing circuit 12, which includes a speech CODEC 16, 116 and a signal processing circuit 18, 118, and the output thereof is coupled to the modulator 4, 120. The radio equipment includes a CPU 14, 180 for controlling the operation of the equipment. Thus, the reference teaches away from the same processor providing data to be transmitted and control signals for controlling the start of a clock or turning off a circuit device.

Therefore, Moriyama fails to disclose or suggest a microprocessor having a control signal output and a data output for output of digital data to be transmitted, combined with a converter coupled to the microprocessor data output for converting the digital data output from the microprocessor into digital packet data to be transmitted by the system, as now claimed. Further, the reference neither discloses nor suggests the clock switch having an input coupled to the control signal output of the microprocessor for receiving a command therefrom to start the local oscillator to generate the first clock signal, as now claimed. The reference also neither discloses nor suggests a transmitter connected to an output of the converter for receiving the digital packet data and being coupled to the local oscillator for use of the first clock signal as an RF carrier for the digital packet data to be transmitted by the transmitter, as claimed. Additionally, Moriyama does not disclose or suggest the microprocessor signaling the crystal oscillator to stop generating the first clock signal, the converter to shut down or the transmitter to shut down, after the RF signal is transmitted, as now claimed.

As the combination of Haban and Moriyama fail to disclose or suggest the concatenation of limitations that define the invention of the subject Patent Application, as now claimed, they cannot make obvious that invention. Neither Tian nor Yamazaki et al., either alone or in combination, overcome the deficiencies of Haban combined with Moriyama, and thus their inclusion in the references relied upon by the Examiner still fails to make obvious Claims 1, 14 and 16. The Claims respectively dependent on Claims 1, 14, and 16 are believed to add further patentably distinct limitations, but are at least patentably distinct for the same reasons as the independent claim upon which they are dependent.

For all of the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

If there are any further charges associated with this filing, the Honorable Commissioner for Patents is hereby authorized to charge Deposit Account #18-2011 for such charges.

Respectfully submitted,
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